What is claimed is:

1. A method for forming a metallization layer outwardly from a semiconductor substrate, the method comprising the steps of:

forming a first layer of a material outwardly from the semiconductor substrate;

forming contact vias that extend through the first layer to the semiconductor substrate;

forming a layer of a second material outwardly from the first layer;

selectively removing portions of the second layer such that the remaining portion of the second layer defines the layout of the metallization layer and the contact vias;

placing the first and second layers at different surface potentials;

electro-depositing the first and second layers in a solution of metal ions by applying a bi-polar modulated voltage having a positive duty cycle and a negative duty cycle, the voltage and surface potentials selected such that the metal is deposited on the remaining portions of the second layer and that metal deposited on the first layer during a positive duty cycle is removed from the first layer during a negative duty cycle; and

selectively removing exposed portions of the first layer.

2. The method of claim 1, wherein the step of depositing a first layer comprises depositing a layer of poly-silicon outwardly from the semiconductor substrate.

3. The method of claim 1, wherein the step of electroplating comprises the steps of:

depositing the semiconductor substrate in an electrolytic bath containing a metal having a reduction potential; and

exposing the bath to a modulated voltage such that during a positive duty cycle the metal is deposited on exposed surfaces of the first layer and the second layer and that during a negative duty cycle the metal is removed from the exposed surface of the first layer.

4. The method of claim 1, wherein the step of depositing a second layer comprises depositing a layer of titanium nitride.

5. The method of claim 3, wherein the step of depositing the semiconductor substrate in an electrolytic bath comprises the step of depositing the semiconductor substrate in an electrolytic bath containing copper ions.

6. The method of claim 1, wherein the step of placing the first and second layers at different surface potentials comprises the step of applying a first voltage to a surface of the first layer and applying a second voltage, different than the first voltage, to the second layer, wherein the first and second layers are separated by an insulating layer.

7. The method of claim 1, wherein the step of placing the first and second layers at different surface potentials comprises the step of selecting a material for the first layer that has an innate surface potential that is less than the innate surface potential for the material selected for the second layer.

8. The method of claim 1, wherein the step of electroplating the first and second surfaces comprises the step of electroplating the first and second surfaces with a voltage source that produces a substantially square wave voltage output.

9. A method for forming a metallization layer outwardly from a semiconductor substrate, the method comprising the steps of:

forming a first layer of a material outwardly from the semiconductor substrate, the first layer having a first innate surface potential;

forming contact vias that extend through the first layer to the semiconductor substrate;

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forming a layer of a second material outwardly from the first layer so as to line the contact vias and cover the first layer, the second layer having a second innate surface potential different from said first innate surface potential;

selectively removing portions of the second layer such that the remaining portion of the second layer defines the layout of the metallization layer and the contact vias;

placing the semiconductor substrate with the first and second layers in an electrolytic bath comprising a solution of metal ions;

applying a bi-polar modulated voltage having a positive duty cycle and a negative duty cycle to the electrolytic bath, the voltage and surface potentials selected such that the metal is deposited on the remaining portions of the second layer and that metal deposited on the first layer during a positive duty cycle is removed from the first layer during a negative duty cycle; and

selectively removing exposed portions of the first layer.

10. The method of claim 9, wherein the step of depositing a first layer comprises depositing a layer of poly-silicon outwardly from the semiconductor substrate.

11. The method of claim 9, wherein the step of placing the semiconductor substrate with the first and second layers in an electrolytic bath comprises the step of placing the semiconductor substrate with the first and second layers in an electrolytic bath containing copper ions in solution.

12. The method of claim 9, wherein the step of depositing a second layer comprises depositing a layer of titanium nitride.

13. The method of claim 9, and further comprising the step of imposing an external voltage to one of the first and second layers to place the first and second layers at different surface potentials.

14. The method of claim 9, and further comprising the step of placing the first and second layers at different surface potentials by applying a first voltage to a surface of the first layer and applying a second voltage, different from the first voltage, to the second layer, wherein the first and second layers are separated by an insulating layer.

15. The method of claim 9, wherein the step of electroplating the first and second surfaces comprises the step of electroplating the first and second surfaces with a voltage source that produces a substantially square wave voltage output.

16. An integrated circuit, comprising:

a plurality of semiconductor devices formed on a semiconductor substrate;

a metallization layer formed outwardly from the semiconductor substrate that selectively interconnects the semiconductor devices so as to be operable to perform a function;

a first patterned layer of material formed outwardly from the semiconductor substrate that matches the metallization pattern; and

a second patterned layer of material, formed between the metallization layer and the first patterned layer, that matches the metallization pattern and lines contact vias that extend through the first layer to the semiconductor substrate.

17. The integrated circuit of claim 16, wherein the metallization layer comprises copper deposited on the second layer in an electrolytic bath.

18. The integrated circuit of claim 16, wherein the first layer comprises poly-silicon.

19. The integrated circuit of claim 16, wherein the second layer comprises titanium nitride.

20. The integrated circuit of claim 16, wherein the metallization layer comprises copper.

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